CIO-DAC08/16
and
CIO-DAC16/16

User's Manual

Revision 6
April, 2001

MEGA-FIFO, the CIO prefix to data acquisition board model numbers, the PCM prefix to data acquisition board model numbers, PCM-DAS08, PCM-D24C3, PCM-DAC02, PCM-COM422, PCM-COM485, PCM-DMM, PCM-DAS16D/12, PCM-DAS16S/12, PCM-DAS16D/16, PCM-DAS16S/16, PCI-DAS6402/16, Universal Library, *Insta*Cal, *Harsh Environment Warranty* and Measurement Computing Corporation are registered trademarks of Measurement Computing Corporation.

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1.0 INTRODUCTION

The CIO-DAC16/16 is a 16-channel analog output board. The CIO-DAC08/16 is an 8-channel analog output board. The analog outputs are from AD660BNs with each output buffered by an OP-27.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. The control register is double buffered so the DAC's output is not updated until the second byte (the high byte) has been written.

The analog outputs may also be set for simultaneous update by selecting XFER on jumper J18. This jumper applies to all DACs.

When the DACs are set for simultaneous update, writing new digital values to a DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ from the board's addresses (any address from base + 0 through base + 31, or through base +15 for the DAC08).

2.0 SOFTWARE INSTALLATION

The CIO-DAC##/16 is supplied with *Insta*Cal. InstaCal is an installation, calibration and test package. Use it to guide the installation procedure. InstaCal also creates a configuration file required for programmers who have purchased the Universal Library programming libraries. Refer to the Software Installation Manual for complete instructions. If you decide not to use *Insta*Cal as a guide, the information required for configuring the board is provided in the following section.

3.0 HARDWARE INSTALLATION

The CIO-DAC16/16 and DAC08/16 each has one bank of range jumpers, a single unipolar/bipolar jumper, one base address switch and a simultaneous update jumper which must be set before installing the board in your computer. The InstaCal program included with both boards shows how these switches are set. *Run this program before you open your computer.*

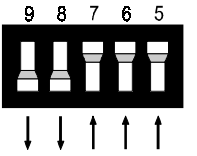
> *We recommend you perform the software installation described in sections below prior to installing the board in your computer. The* ***InstaCal™*** *program provided will show you how to properly set the switches and jumpers on the board prior to physically installing the board in your computer.*

The CIO-DAC16/16 is setup at the factory with:

BASE ADDRESS	300h (768 decimal)
SIMULTANEOUS UPDATE	In the UPDATE position. Single channel update.
ANALOG OUTPUT	±5V
UNI / BIP JUMPER	BIP

3.1 BASE ADDRESS

Unless there is already a board in your system which uses address 300h (768 decimal) leave the switches as they are set at the factory. The base address switch for the CIO-DAC16/16 is shown here, set to 300 hex. The CIO-DAC08/16 has one additional switch on the base address switch bank (A4 with a weight of 10 hex).



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20

Figure 3-1. Base Address Switches (Set to 300h)

The address switches may be set for a base address in the range of 000-3E0 (3F0 for the DAC08) so it should not be hard to find a free address area. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31Fh are free to use. Addresses not specifically listed, such as 390-39F, are free.

Refer to table 3-1 for PC I/O address usage.

Table 3-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

3.2 ANALOG OUTPUT RANGE JUMPERS

The analog output voltage range of each channel is set with a jumper. The jumpers are located on the board directly below the calibration potentiometers and are labeled J1 through J8 on the DAC08 and. J1 through J16 on the DAC16.

Set the jumpers for an individual channel as shown in Figure 3-2.

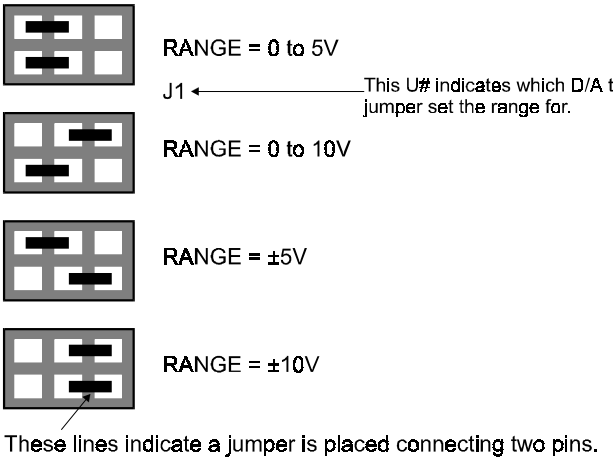

RANGE = 0 to 5V
J1
This U# indicates which D/A this jumper set the range for.
RANGE = 0 to 10V
RANGE = ±5V
RANGE = ±10V
These lines indicate a jumper is placed connecting two pins.

Figure 3-2. Range Jumpers

The available ranges are:

0 to 5V (Unipolar)
0 to 10V (Unipolar)
±5V (Bipolar)
±10V (Bipolar)

3.3 UNIPOLAR/BIPOLAR INITIAL ZERO STATE JUMPER

The CIO-DAC16/16 and DAC08/16 boards have a unipolar/bipolar jumper which selects the unipolar/bipolar initial zero state of the DAC output on either power-up or reset. There is a single jumper for the entire board (Figure 3-3). This jumper is located near the ISA bus connector.

At power-up, the value in the DACs will be set according to Table 3-2.

Table 3-2. DAC Initial States at Power-up

State of UNI/BIP Jumper	DAC Code	IF DAC set for Unipolar Output	If DAC set for Bipolar Output
UNI	0	0.000	Minus Full Scale
BIP	32768	Mid Scale	0.000

This jumper affects ONLY the power-up / reset condition of the DACs. It is here to insure that when the computer is turned on, or, if the computer is reset, process controls will come up in a known, safe state.

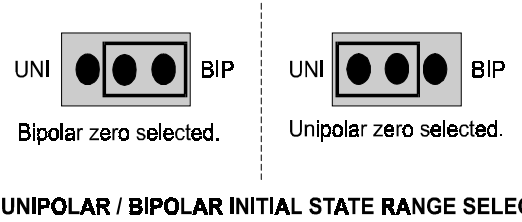


Figure 3-3. Initial State Range Select Jumper Positions

If your application requires that the output of all DACs maintain a zero state initially, you should use simultaneous update mode. This mode allows you to set the value stored in the output registers before the output voltage is updated. If individual update mode is used, the value of all DAC outputs will be updated to whatever value is stored in the output registers at the moment that the first DAC is updated. This value is undefined but typically will be + full scale (register value = FFFFh).

Using the simultaneous mode allows you to set the values of all registers before any of the DACs are updated to the register value.

3.4 SIMULTANEOUS UPDATE JUMPER

This jumper selects either individual DAC update when the MSB register is written (UPDATE) or simultaneous transfer of data to all DAC outputs on a read (XFER). In simultaneous transfer mode, new output data is loaded into the DAC registers, but the DAC outputs do not change until one of the registers have been read. The simultaneous update occurs whenever any of the CIO-DAC16/16 addresses BASE + 0 through BASE + 31 (or addresses BASE + 0 through BASE + 15 for the DAC08) are read (Figure 3-4).

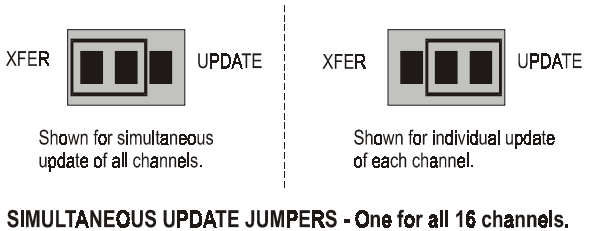


Figure 3-4. Simultaneous Update Jumper

Note: Use simultaneous update to maintain power-up state (see section on "Initial Zero State Jumper").

In this way, the CIO-DAC16/16 and DAC08/16 may be set to hold new values until all channels are loaded, then update all sixteen simultaneously. This can be a very useful feature for multi-axis motor control.

3.5 INSTALLING THE BOARDS IN THE COMPUTER

1. Turn the power off.
2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.
3. Locate an empty expansion slot in your computer.
4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard or your board.

3.6 CABLING TO THE BOARD

The CIO-DAC16/16 and the DAC08/16 connectors are accessible through the PC/AT expansion bracket. The connector is a standard 37-pin, D-type male connector. A mating female connector, such as the C37FF-2, is available from Measurement Computing.

Several cabling and screw termination options are available.

Table 3-3. Cable Termination Options

DFCON-37	D connector, D shell and termination pins to construct your own cable.
C37FF-2	Two-foot (and longer) ribbon cable with 37-pin D connectors.
C37FFS-5	Five-foot shielded round cable with molded ends housing 37-pin connectors. Also available in 10-ft. length.
CIO-MINI37	Simple, 40-position, 4" x 4" screw terminal board.
CIO-TERMINAL	Full featured 4" x 16" screw terminal board with prototyping and interface circuitry.

3.7 SIGNAL CONNECTION

The analog outputs of the CIO-DAC16/16 and the DAC08/16 are two-wire hook-ups; a signal, labeled D/A # OUT on the connector diagram after this section, and a Low Level Ground (LLGND). The low level ground is an analog ground and is the ground reference which should be used for all analog hook-ups.

Possible analog output ranges are:

Bipolar Ranges	±10V	±5V
and		
Unipolar Ranges	0 to 10V	0 to 5V

Each of the DAC outputs are individually buffered through an OP-27 operational amplifier (OP-AMP). The OP-27s are socketted so that if one goes bad it can be replaced in the field. The OP-27 for each channel is located just below the calibration potentiometers for that channel.

Each channel is capable of sinking or sourcing ±5 mA. That means a load of 2K Ohms can be connected to each channel at the full rated output swing of +10V.

As the load resistance is raised from 2K up to 10 MegΩ or more, the output load on the DAC decreases. Any resistance greater than 2K is acceptable.

As the load resistance decreases, the output load increases. The OP-27 responds by producing a lower output voltage. If your DAC board will not produce the output voltage specified by the code & range combination, check the load with an ohmmeter.

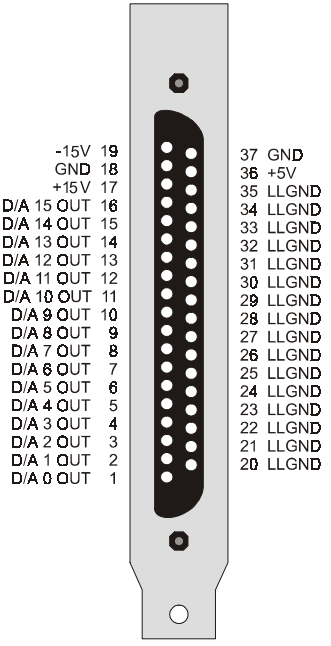
Under normal circumstances you will not damage the OP-27 by connecting the output to ground. If your connection results in a failure of the OP-27, chances are good that there was some potential at the connecting point in addition to a load at ground or between 0 and 2K ohms. Explore the point with a DVM before reconnecting the CIO-DAC16/16 or DAC08/16 (and after replacing the OP-27 of course). Connect the negative lead of the DVM to any LLGND pin of the CIO-DAC16/16 or DAC08/16.

3.8 CONNECTOR DIAGRAM

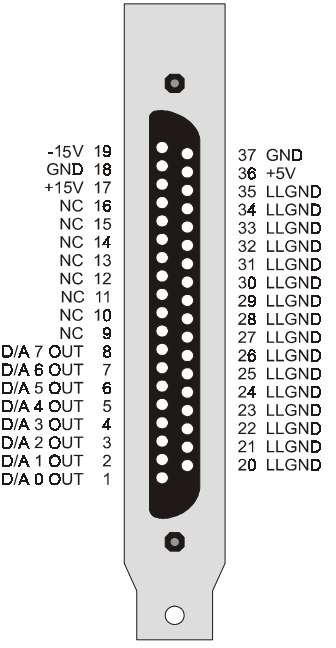
Both the CIO-DAC16/16 and DAC08/16 are 37 pin D type connectors accessible from the rear of the PC through the expansion backplate.

The connector accepts female 37-pin, D-type connectors, such as those on the C37FF-2, a 2-foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL, CIO-SPADE50 and CIO-MINI37 screw terminal boards in the Measurement Computing catalog.



CIO-DAC16/16 CONNECTOR



CIO-DAC08/16 CONNECTOR

4.0 REGISTER ARCHITECTURE

The CIO-DAC16/16 and DAC08/16 are simple boards to understand right down to their lowest level. All control and data is read/written with simple I/O read and write signals. No interrupt or DMA control software is required. Thus, the board's functions are easy to control directly from BASIC, C or PASCAL.

4.1 CONTROL & DATA REGISTERS

The CIO-DAC16/16 has 32 analog output registers, the CIO-DAC08/16 has 16. There are two for each channel, one for the lower eight bits and one for the upper eight bits.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the bit weights in Table 4-1 apply:

Table 4-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.
The method of programming required to set/read bits from bytes is beyond the scope of this manual. Refer to a basic book on programming.

In summary form, the registers and functions are listed in Table 4-2. Each register has eight bits which may constitute a byte of data or eight individual bit functions.

Table 4-2. Register Summary

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous update.
BASE + 1	D/A 0 Most Significant Byte	Initiate simultaneous update.
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous update.
BASE + 3	D/A 1 Most Significant Byte	Initiate simultaneous update.
BASE + 4	D/A 2 Least Significant Byte	Initiate simultaneous update.
BASE + 5	D/A 2 Most Significant Byte	Initiate simultaneous update.
BASE + 6	D/A 3 Least Significant Byte	Initiate simultaneous update.
BASE + 7	D/A 3 Most Significant Byte	Initiate simultaneous update.
BASE + 8	D/A 4 Least Significant Byte	Initiate simultaneous update.
BASE + 9	D/A 4 Most Significant Byte	Initiate simultaneous update.
BASE + 10	D/A 5 Least Significant Byte	Initiate simultaneous update.
BASE + 11	D/A 5 Most Significant Byte	Initiate simultaneous update.
BASE + #	And so on for each DAC	Same.

The DAC16 contains 32 registers (16 register pairs). The DAC08 contains 16 registers. Each register pair controls 1 D/A output.

Each DAC has two 8-bit registers which are used to control it. The first register contains the least significant eight bits of D/A code and should be written first.

7	6	5	4	3	2	1	0
D8	D9	D10	D11	D12	D13	D14	LSB

The second register contains the most significant eight bits of D/A code and should be written to last. A write to this register will update the output of the D/A with all 16 bits of the D/A code contained in the two registers. If the simultaneous update jumper is set for XFER, no update will occur until a read of any one of the DAC registers is executed. Upon a read, all DACs will update together.

7	6	5	4	3	2	1	0
MSB	D1	D2	D3	D4	D5	D6	D7

4.2 OUTPUT TRANSFER FUNCTIONS

To program a DAC, you must select the output you desire in volts, then apply a transfer function to that value. The transfer function for code = output is:

The UNIPOLAR transfer function of the DAC is:

FSV / 65,536 * CODE = OutV or CODE = OutV / FSV * 65,536

For Example:

If the range is 0 to 5V	CODE = 2/5 * 65,536
and you desire a 2V output.	CODE = 26,214

The BIPOLAR transfer function for the DAC is:

FSV/65,536 * CODE – 0.5 * FSV or CODE = (OutV + 0.5 * FSV) / FSV * 65,536

For example:

If the range is set to ±10	CODE = (–7V + 0.5 * 20) / 20 * 65,536
and you desire a –7V output.	CODE = 9,830

5.0 SPECIFICATIONS

Power Consumption

+5V supply	
CIO-DAC16/16	1.8A typical, 2.25 max
CIO-DAC08/16	1.3A typical, 1.7A max

Analog Output

Resolution	16 bits
Number of channels	
CIO-DAC16/16	16 Voltage Output
CIO-DAC08/16	8 Voltage Output
D/A type	AD660BN
Voltage Ranges	±5V, ±10V, 0 to 5V, 0 to 10V, jumper selectable
Offset error	Adjustable to zero
Gain error	Adjustable to zero
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	Guaranteed monotonic to 15 bits over temperature
Gain drift (DAC)	±15 ppm/°C max
Bipolar offset drift (DAC)	±5 ppm/°C max
Unipolar offset drift (DAC)	±3 ppm/°C max
Throughput	System dependant
Slew Rate	2.8 V/µS Typical
Settling time (20V step to .0008%)	12µs typ, 19us max
Settling time (10V step to .0008%)	6µs typ, 9us max
Current Drive	±5 mA min
Output resistance (OP-27)	0.1 ohm max
Output short-circuit duration	40 mA min Continuous
Miscellaneous	Double buffered output latches Update DACs individually or all DACs simultaneously (jumper selectable) Power up and reset, all DAC's cleared to 0 volts (jumper selects bipolar or unipolar zero)

Environmental

Operating temerature range	0 to 70°C
Storage temerature range	-40 to 100°C
Humidity	0 to 90% non-condensing

For your notes.

For your notes.

EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

Part Number	Description
CIO-DAC16/16	16 Channel analog output board
CIO-DAC08/16	8 Channel analog output board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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